

Customer No.: 31561  
Application No.: 10/711,509  
Docket No.: 12405-US-PA-0P

**AMENDMENT**

Please amend the application as indicated hereafter.

**To the Claims**

Claim 1. (currently amended) A manufacturing method of a thin film transistor (TFT), comprising:

forming a gate over a substrate;

forming an inter-gate dielectric layer over the substrate covering the gate;

forming a channel layer over a portion of the inter-gate dielectric layer at least over the gate, wherein the channel layer is a lightly doped amorphous silicon layer, and the step of forming the channel layer comprises:

forming a first lightly doped sub-amorphous silicon layer over the portion of the inter-gate dielectric layer at a first deposition rate; and

forming a second lightly doped sub-amorphous silicon layer over the first lightly doped sub-amorphous silicon layer at a second deposition rate; and

forming source/drain regions over the channel layer, wherein the source/drain regions are separated by a distance, ~~and the lightly doped amorphous silicon layer between the source region and the drain region is a channel region.~~

Claim 2. (original) The manufacturing method of claim 1, wherein the channel layer comprises an N-type lightly doped amorphous silicon layer.

Claim 3. (original) The manufacturing method of claim 1, wherein the channel layer comprises a P-type lightly doped amorphous silicon layer.

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**Claim 4. (original)** The manufacturing method of claim 1, wherein the channel layer is doped with phosphorous atoms, and a concentration of phosphorous atoms is in a range of about 1E17 atom/cm<sup>3</sup> to about 1E18 atom/cm<sup>3</sup>.

**Claim 5. (original)** The manufacturing method of claim 1, wherein the channel layer is doped with boron atoms, and a concentration of boron atoms is in a range of about 1E16 atom/cm<sup>3</sup> to about 5E17 atom/cm<sup>3</sup>.

**Claim 6. (original)** The manufacturing method of claim 1, wherein the step of forming the channel layer comprises performing a chemical vapor deposition (CVD) process using a reaction gas mixture comprising silane (SiH<sub>4</sub>), hydrogen (H<sub>2</sub>) and phosphine (PH<sub>3</sub>), wherein an effective content ratio of the phosphine (PH<sub>3</sub>) is in a range of about 2.8E-7 to about 8E-6, and wherein the effective content ratio of the phosphine (PH<sub>3</sub>) is equal to the ratio of the content of phosphine (PH<sub>3</sub>) to the total content of silane (SiH<sub>4</sub>), hydrogen (H<sub>2</sub>) and phosphine (PH<sub>3</sub>).

**Claim 7. (original)** The manufacturing method of claim 1, wherein the step of forming the channel layer comprises performing a chemical vapor deposition (CVD) process using a reaction gas mixture comprising silane (SiH<sub>4</sub>), hydrogen (H<sub>2</sub>) and boroethane (B<sub>2</sub>H<sub>6</sub>), wherein an effective content ratio of the boroethane (B<sub>2</sub>H<sub>6</sub>) is in a range of about 5E-7 to about 1E-5, and wherein the effective content ratio of the boroethane (B<sub>2</sub>H<sub>6</sub>) is equal to the ratio of the content of boroethane (B<sub>2</sub>H<sub>6</sub>) to the total content of silane (SiH<sub>4</sub>), hydrogen (H<sub>2</sub>) and boroethane (B<sub>2</sub>H<sub>6</sub>).

**Claim 8. (cancelled)**

**Claim 9 (cancelled)**

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Claim 10. (original) The manufacturing method of claim 1, further comprising a step of forming a protection layer over the substrate after the step of forming the source/drain regions covering the source/drain regions, the channel layer and the inter-gate dielectric layer.

**Claims 11-18 (cancelled)**

Claim 19 (currently amended) A manufacturing method of a thin film transistor (TFT), comprising:

forming a gate over a substrate;  
forming an inter-gate dielectric layer over the substrate covering the gate;  
forming a channel layer over a portion of the inter-gate dielectric layer at least over the gate, wherein the channel layer comprises a lightly doped amorphous silicon layer and the step of forming the channel layer comprises:  
forming a first lightly doped sub-amorphous silicon layer over the portion of the inter-gate dielectric layer at a first deposition rate; and  
forming a second lightly doped sub-amorphous silicon layer over the first lightly doped sub-amorphous silicon layer at a second deposition rate;  
forming an ohmic contact layer over the channel layer; and  
forming source/drain regions over the channel layer, wherein the source/drain regions are separated by a distance, ~~and the lightly doped amorphous silicon layer between the source region and the drain region is a channel region.~~

Claim 20. (previously presented) The manufacturing method of claim 19, wherein the channel layer comprises an N-type lightly doped amorphous silicon layer.

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**Claim 21. (previously presented)** The manufacturing method of claim 19, wherein the channel layer comprises a P-type lightly doped amorphous silicon layer.

**Claim 22. (previously presented)** The manufacturing method of claim 19, wherein the channel layer is doped with phosphorous atoms, and a concentration of phosphorous atoms is in a range of about 1E17 atom/cm<sup>3</sup> to about 1E18atom/cm<sup>3</sup>.

**Claim 23. (previously presented)** The manufacturing method of claim 19, wherein the channel layer is doped with boron atoms, and a concentration of boron atoms is in a range of about 1E16 atom/cm<sup>3</sup> to about 5E17 atom/cm<sup>3</sup>.

**Claim 24. (previously presented)** The manufacturing method of claim 19, further comprising a step of forming a protection layer over the substrate after the step of forming the source/drain regions covering the source/drain regions, the channel layer and the inter-gate dielectric layer.

**Claim 25. (cancelled)**

**Claim 26. (previously presented)** The manufacturing method of claim 19, wherein the step of forming the channel layer comprises performing a chemical vapor deposition (CVD) process using a reaction gas mixture comprising silane (SiH<sub>4</sub>), hydrogen (H<sub>2</sub>) and phosphine (PH<sub>3</sub>), wherein a effective content ratio of the phosphine (PH<sub>3</sub>) is in a range of about 2.8E-7 to about 8E-6, and wherein the effective content ratio of the phosphine (PH<sub>3</sub>) is equal to the ratio of the content of phosphine (PH<sub>3</sub>) to the total content of silane (SiH<sub>4</sub>), hydrogen (H<sub>2</sub>) and phosphine (PH<sub>3</sub>).

**Claim 27. (previously presented)** The manufacturing method of claim 19, wherein the step of forming the channel layer comprises performing a chemical vapor deposition

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(CVD) process using a reaction gas mixture comprising silane ( $\text{SiH}_4$ ), hydrogen ( $\text{H}_2$ ) and boroethane ( $\text{B}_2\text{H}_6$ ), wherein a effective content ratio of the boroethane ( $\text{B}_2\text{H}_6$ ) is in a range of about 5E-7 to about 1E-5, and whercin the effective content ratio of the boroethane ( $\text{B}_2\text{H}_6$ ) is equal to the ratio of the content of boroethane ( $\text{B}_2\text{H}_6$ ) to the total content of silane ( $\text{SiH}_4$ ), hydrogen ( $\text{H}_2$ ) and boroethane ( $\text{B}_2\text{H}_6$ ).